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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/854,491	05/15/2001	Thomas Sean Houlihane	550-229	7919

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NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
PROCTOR, JASON SCOTT	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 10/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/854,491	HOULIHANE ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

In the previous Office Action, claims 1-49 were rejected.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6 June 2006 has been entered.

Claims 1, 15, 17, 19, 31, 32, 34, 35, 39-41, 43, and 44 have been amended. Claims 1-49 are pending in this application.

Claims 1-49 are rejected.

Claim Rejections – 35 USC § 101

The previous rejections under 35 U.S.C. § 101 of claims 34 and 43 have been withdrawn in response to Applicants' amendments.

Response to Arguments

Applicants' arguments and remarks regarding the previous rejections under 35 U.S.C. §§ 102 and 103 have been fully considered. In response, and in response to the amendments to the claims, the previous rejections under 35 U.S.C. § 102 of claims 1-5, 12-14, 16-21, 28-30, 32-34, 35-37, and 41-43 as being anticipated by Gupte have been withdrawn. Also, the rejections under

35 U.S.C. § 103 of claims 15, 31, and 39 as being unpatentable over Gupte in view of Rostoker have been withdrawn.

Applicants remarks regarding the rejections under 35 U.S.C. § 103 of claims 6-11, 22-27, and 44-49 have been fully considered, however reconsideration of the claims and the references necessitates the new grounds of rejection set forth below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

1. Claims 1-7, 12-23, and 28-45 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 5,903,475 to Gupte et al. (Gupte) in view of "Developing an EDA Vendor-Independent ASIC System for VHDL" by Bob Holstine and Greg Haynes (Holstine).

Regarding claim 1, Gupte teaches

Conducting a simulation of a data processing apparatus performing a test sequence of data processing operations [*"generating a programming language capture module that captures inputs to and outputs from the integrated circuit during system simulation,"* (column 2, lines 23-33)], including simulating operation of both a subsystem under test and one or more surrounding circuits [*"system simulation"* (column 2, lines 2-22); also (column 9, lines 22-34; column 9, lines 22-34)];

recording input signals to and output signals from said subsystem circuit while performing said test sequence of data processing operations [*"The Vector Capture program generates the capture module which is an HDL file that is utilized during a system simulation to capture the input and output vectors around the ASIC."* (column 10, lines 6-9); *"At step 462, the system generates code to capture outputs on each strobe edge. The system generates code to open a single input file and one output file for each output. At step 466, the system generates code to capture inputs on change and the capture module has been generated."* (column 10, lines 25-29); also (column 2, lines 7-22; column 6, lines 53-64; column 9, lines 18-21)]; and

using at least representation of recorded input signals to form a reduced model to replay recorded input signals to subsystem circuit model and to apply a plurality of sampling rules to said output signals to sample said output signals to detect changes and times of changes in said output signals and to compare said output signals with at least one predetermined characteristic indicative of correct operation [*"The stand-alone simulation generates output test vectors 366. Verifying the representation of the ASIC entails comparing the "golden" vectors to the test vectors. If the golden and test vectors are identical, then the representation of the ASIC used during stand-alone simulation is the same as the customers original behavioral model."* (column 9, lines 30-41); also (column 2, lines 7-22; column 6, lines 41-52); regarding sampling rules, see (column 8, line 49 – column 9, line 8)];

whereby a subsystem under test and reduced model may be used to simulate the subsystem under test performing the test sequence of data processing operations without simulating operation of one or more surrounding circuits [*"Thus, the customer's system simulation is reproduced without having to reproduce the customer's system environment which allows the operation of the ASIC to be verified during various states of synthesis."* (column 8, lines 36-40); also (column 2, lines 7-22; column 6, lines 41-64)].

Gupte does not expressly teach recording input signals to and output signals from said subsystem circuit **in response to changes in at least one of said input signals and said output signals**.

Holstine teaches recording input signals to and output signals from a subsystem circuit in response to changes in at least one of said input signals and said output signals [*"...we use the VHDL standard TEXTIO package to write simulation output to a text file in a print-on-change format. Writing this output is accomplished using a VHDL module that we call 'a monitor.' All of the primary ports of a design are input to the monitor, and their values are printed to a text file whenever the value of any port changes. For bi-directional ports, the monitor writes the input and output components of the signal, as required test-program generation."* (page 2 of 7, first full paragraph)].

Holstine and Gupte are analogous art because both are drawn to circuit simulation.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the "print-on-change" format of writing simulation output with the method taught by Gupte for storing "golden vectors". Motivation is expressly found in Holstine, such as to achieve EDA vendor neutrality [*"Writing a print-on-change file in text format is generally less efficient than using the native database capabilities of the simulator, but it has the advantage of being completely independent of an EDA vendor. This means a VHDL ASIC-design system can be developed without making modifications for a wide range of VHDL simulators."* (page 2 of 7, second full paragraph)].

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Holstine with the teachings of Gupte to arrive at the invention as specified in claim 1.

Regarding claim 2, Gupte teaches the use of a configuration file including data specifying input signals, output signals, and bi-directional signals exchanged with the subsystem circuit in order to form the reduced model [*"bidirect enable definitions"* (column 8, line 44 – column 9, line 8)].

Regarding claim 3, Gupte teaches that signals from the subsystem are used to determine when bi-directional signals can be driven making allowance for variations in delays inherent in output loads [*"The input and output for an inout are combined using the associated BDENABLE signal which specifies whether the inout is an input or an output. Code is generated that assigns the inout to the input wire or the output wire depending on the value of the input test signal."* (column 10, lines 11-17)].

Regarding claim 4, Gupte teaches that the reduced model includes a rule having an output signal time window within which a change in said output signal to a predetermined output signal value should occur to be indicative of correct operation [*"The strobes section specify the appropriate time to capture expected vectors. In the sample IOS file, all outputs are assumed to be synchronous and periodical such that the line 'strobe strb1 period 20 start 19 stop 0 outputs pout dav dbus' will instruct the simulators to extract output vectors every 20 ns on the signals pout, dav and dbus starting 19 ns into the cycle."* (column 8, line 44 – column 9, line 8)].

In response to the previous rejection and interpretation of Gupte, Applicants argue primarily that:

> This specification of specific precise times at which sampling occurs is not the same as specifying "an output signal time window" as set out in Applicants' dependent claim 4.

The Examiner respectfully traverses this argument as follows.

Applicants allegation that the Gupte reference does not anticipate this limitation is insufficient to overcome the rejection as established in the prosecution record. The Gupte reference clearly describes an exemplary "time window" of 20 ns. Further, Gupte characterizes this as "specify[ing] the appropriate time to capture expected vectors" (column 8, line 66 – column 9, line 2). The Gupte reference clearly describes "golden vectors" that are indicative of correct operation.

Applicants' arguments have been fully considered but have been found unpersuasive.

Regarding claim 5, Gupte teaches recording output signals from a subsystem circuit under test (column 8, line 44 – column 9, line 8). While Gupte et al. does not explicitly disclose that the output signals values are one of: high; low; changed; and high impedance, it is inherent that signals in a digital circuit are referred to by the values in the enumerated group or by equivalent terms. Therefore, by recording output signals, the invention of Gupte records values which are one of: high; low; changed; and high impedance.

Regarding claim 6, Gupte teaches that within said data processing apparatus at least one of said output signals is a strobe output signal [*"The IOS file contains the I/O specifications of the ASIC. The IOS file consists of three parts: port definitions, strobes, and bidirect enable definitions."* (column 8, lines 44-50)] used to trigger sampling of at least one strobed output signal [*"...the line "strobe strb1 period 20 start 19 stop 0 outputs pout dav dbus" will instruct the simulators to extract output vectors every 20 ns on the signals pout, dav and dbus starting 19*

ns into the cycle" (column 9, lines 2-8)], said reduced model including a rule whereby a change in said strobe output signal is detected and used to verify the correct state of said at least one strobed output signal [*"The strobes section specify the appropriate time to capture expected vectors."* (column 8, line 44 – column 9, line 8)].

Several statements regarding the Gupte reference made by the Examiner in the final Office Action at pages 12-13 have been reconsidered. These previous statements were based upon a misinterpretation of the claim language and the Gupte reference. The Examiner apologizes for any inconvenience this may cause.

Applicants' remarks have been fully considered by the Examiner. However, in light of the new grounds of rejection for claim 6, these arguments have been found unpersuasive.

Regarding claim 7, Gupte teaches a rule that includes a strobe output signal time window within which a change in said strobe output signal to a predetermined strobe output signal value should occur to be indicative of correct operation [(column 8, line 44 – column 9, line 8); *"The stand-alone simulation generates output test vectors 366. Verifying the representation of the ASIC entails comparing the "golden" vectors to the test vectors."* (column 9, lines 33-41)].

Regarding claim 12, Gupte teaches that the full subsystem circuit model from which said input signals and said output signals are recorded may be different from that to which said input signals are subsequently replayed and from which output signals are subsequently analysed [*"During system simulation, the invention captures 'golden' vectors that may be used to test the ASIC during stand-alone simulation... Thus, the customer's simulation system is reproduced*

without having to reproduce the customer's system environment which allows the operation of the ASIC to be verified during various states of synthesis." (column 2, lines 7-22); *"The stand-alone simulation reproduces the customers system simulation without having to reproduce the customer's system environment."* (column 9, lines 22-34)].

Regarding claim 13, Gupte teaches that the full subsystem circuit model may change between different versions during regression testing [*"The design configuration managers maintain versions of the design information and security for modification of the design information."* (column 17, lines 14-25); *"The system then issues a command to check out the HDL code for the requested design version from the design configuration manager at step 1002."* (column 18, lines 19-24)].

Regarding claim 14, Gupte teaches that the full subsystem circuit may change between being one of an RTL model, a netlist model, or other software views [*"Additionally, the Capture may be utilized to test the generation of a gate level model from an RTL model... The outputs are compared to verify that the gate level model is an accurate depiction of the ASIC."* (column 9, lines 42-46)].

Regarding claim 15, Gupte teaches that changes in at least one of said output signals other than at sampling instants of a corresponding one of said sampling rules for that output signal are also monitored (column 8, line 44 – column 9, line 8). Alternatively, Holstine teaches

that output signals other than at sampling instants of a corresponding one of said sampling rules for that output signal are also monitored (page 2 of 7, first full paragraph).

Regarding claim 16, Gupte teaches recording progress messages for replay during regression testing [*"The system prints statistics at step 414."* (column 9, line 58 – column 10, line 4)]. Statistics are presumed equivalent to progress messages.

Regarding claim 17, the limitations recite an apparatus which performs the method as recited by claim 1. As the invention of Gupte is embodied in a computer (Fig. 2; column 4, lines 5-7), the limitations of claim 17 are rejected for rationale similar to that used in the rejection claim 1 above.

Regarding claim 18, the limitations recite a computer program product comprising a computer program for controlling a computer to perform a method as recited in claim 1. As the invention of Gupte is embodied in a computer (Fig. 2; column 4, lines 5-7), the limitations of claim 18 are rejected for rationale similar to that in the rejection of claim 1 above.

Regarding claims 19, 20-23, and 28-31, the limitations recite a method for modeling a data processing apparatus corresponding to the method for creating a model of a data processing apparatus as recited by claim 1 and further limited by claims 4-7 and 12-15. As the invention of Gupte models a data processing apparatus (column 1, lines 62-65; column 2, lines 7-22), the

limitations of claims 19, 20-23, and 28-31 are rejected for rationale similar to that in the rejection of claims 1, 4-7, and 12-15 above.

Regarding claim 32, the limitations recite an apparatus for modeling a data processing apparatus corresponding to the apparatus for creating a model of a data processing apparatus as recited in claim 17. As the invention of Gupte is embodied in a computer (Fig. 2; column 4, lines 5-7) and performs a simulation of the data processing apparatus (column 1, lines 62-65; column 2, lines 7-22) the limitations of claim 32 are rejected for rationale similar to that in the rejection of claim 17 above.

Regarding claim 33, the limitations recite a computer program product comprising a computer program controlling a computer to perform a method as claimed in claim 19. As the invention of Gupte is embodied in a computer (Fig. 2; column 4, lines 5-7) the limitations of claim 33 are rejected for rationale similar to that in the rejection of claim 19 above.

Regarding claim 34, Gupte software for implementing the method of claim 1 [*"In one embodiment, a computer implemented method of testing integrated circuits..."* (page 2, lines 22032)]. Claim 34 is therefore rejected for rationale similar to that in the rejection of claim 1 above.

Claim 35 recites a combination of limitations found in claims 1 and 4 and is rejected for rationale similar to that given above for claims 1 and 4.

Claims 36 and 37 recite combinations of limitations found in claims 5 and 3, respectively, and is rejected for rationale similar to that given above for claims 5 and 3.

Claim 38 recites limitations found in claim 6 and is rejected for rationale similar to that given above for claim 6.

Claim 39 recites limitations found in claim 15 and is rejected for rationale similar to that given above for claim 15.

Claim 40 recites an apparatus that performs the method of claims 1 and 4. As the invention of Gupte is embodied in a computer (Fig. 2; column 4, lines 5-7) the claim 40 is rejected by rationale similar to that in the rejection of claims 1 and 4 above.

Claim 41 recites an apparatus that performs the method of claims 1 and 4. As the invention of Gupte is embodied in a computer (Fig. 2; column 4, lines 5-7) the claim 43 is rejected by rationale similar to that in the rejection of claims 1 and 4 above.

Claim 42 recites a computer program product that performs the method of claim 35. As the invention of Gupte is embodied in a computer (Fig. 2; column 4, lines 5-7) claim 42 is rejected for rationale similar to that in the rejection of claims 1 and 4 above.

Claim 43 recites limitations found in claim 34 and is rejected for rationale similar to that in the rejection of claim 34 above.

Claims 44 appears to recite the limitations of claim 6 in independent form and is therefore rejected for rationale similar to that given above for claim 6.

Claim 45 appears to recite the limitations of claim 7 and is therefore rejected for rationale similar to that given above for claim 7.

2. Claims 8-11, 24-27, and 46-49 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Gupte in view of Holstine as applied to claim 6 above, and further in view of "SourceModel User's Manual for VHDL" by Synopsys.

Regarding claim 8, neither Gupte nor Holstine expressly teach a rule that include a strobed output signal time window within which said strobed output signal should hold a predetermined strobed output signal value to be indicative of correct operation.

Synopsys teaches a rule that includes a strobed output signal time window within which said strobed output signal should hold a predetermined strobed output signal value to be indicative of correct operation [*"For example, the setup time trs_W_X = 7 ns indicates that the signal W must remain steady for 7 ns before X rises. For another example, the hold time trh_Y_Z = 4 ns indicates that at least 4 ns must elapse after the rising edge of clock Z before the input Y can change."* (page 49, second full paragraph)].

Synopsys and Gupte in view of Holstine are analogous art because all are drawn to circuit simulation.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the VHDL rules taught by Synopsys in the combination of Gupte in view of Holstine. Motivation is expressly taught by Synopsys, such as checking for timing violations in the circuits being simulated [*"Behavioral models also contain properties such as setup time, hold times, and minimum pulse widths so that the simulator can check for violations of these times in the signals propagating through the circuit."* (page 18, fourth paragraph)].

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Synopsys with Gupte in view of Holstine to arrive at the invention specified in claim 8.

Regarding claim 9, Synopsys teaches that a strobed output signal time window is non-symmetrically disposed about a time when said strobe output signal is sampled [*"Many signals go through a high-impedance (Z) or unknown (X) transitional state before entering a valid state (low or high). Hold delays define the time before signal b becomes inactive or active-unknown prior to becoming valid."* (page 50, first full paragraph)].

Regarding claim 10, Synopsys teaches that a strobed output signal time window is at least partially surrounded by a settling time window within which said strobed output signal is permitted to change [*"Figure 8 shows the format of the edge-to-output hold delay (h) parameter.*

For example, a hold delay of thrx_W_Y = 5 ns indicates that signal Y will achieve an unknown state 5 ns after the rising edge of signal W." (page 50, third full paragraph)].

Regarding claim 11, Synopsys teaches that a strobed output signal time window is at least partially surrounded by a settled time window within which said strobed output signal is not permitted to change [*"For example, the setup time trs_W_X = 7 ns indicates that the signal W must remain steady for 7 ns before X rises. For another example, the hold time trh_Y_Z = 4 ns indicates that at least 4 ns must elapse after the rising edge of clock Z before the input Y can change."* (page 48, second full paragraph)].

Claims 24-27 recite a method for modeling a data processing apparatus corresponding to the method for creating a model of a data processing apparatus as recited by claims 8-11. As the combination formed in the rejection of claims 8-11 models a data processing apparatus, as taught by Gupte (column 1, lines 62-65; column 2, lines 7-22), claims 24-27 are rejected for rationale similar to that given above for claims 8-11.

Claims 46-49 appear to recite the limitations of claims 8-11 and are therefore rejected for rationale similar to that given above for claims 8-11.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

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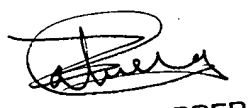

ZOILA CABRERA
PRIMARY EXAMINER
TECHNOLOGY CENTER 2100

10/12/06